I claim:

1. A memory cell array, comprising:

a substrate having a main face;

a first insulating layer configured on said main face of said substrate, said first insulating layer formed with a trench having a bottom and edges;

a first line configured in said trench of said first insulation layer;

a second line;

a memory element configured at a point of intersection between said first line and said second line, said memory element being switched between said first line and said second line;

a first yoke disposed adjacent said bottom and said edges of said trench of said first insulation layer, said first yoke configured such that a magnetic flux through said first yoke is essentially closed in said memory element, said first yoke including a magetizable material with a relative permeability of at least 10; and

a line selected from the group consisting of said first line and said second line being supplied with current during a write access and being partially surrounded by said first yoke.

2. The memory cell array according to claim 1, wherein said first yoke includes a soft-magnetic, ferromagnetic material.

3. The memory cell array according to claim 2, wherein:

said first line has a surface;

said substrate includes a carrier wafer with a main face defining said main face of said substrate; and

said memory element is configured above said first yoke and on said surface of said first line.

4. The memory cell array according to claim 2, wherein:

said substrate includes a carrier wafer with a main face defining said main face of said substrate;

said second line is configured above said memory element and has edges and a surface facing away from said memory element; and

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comprising:

a second yoke configured above said memory element and adjacent said edges of said second line and adjacent said surface of said second line facing away from said memory element; and

a second insulating layer partially surrounding said second line and said second yoke.

5. The memory cell array according to claim 4, wherein said memory element is configured above said first yoke and said first line.

6. The memory cell array according to claim 1, comprising a second yoke configured above said memory element and configured such that a magnetic flux through said second yoke is essentially closed in said memory element; said second yoke including a magetizable material with a relative permeability of at least 10.

7. The memory cell array according to claim 1, comprising:

a plurality of first lines disposed parallel to each other;

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a plurality of second lines disposed parallel to each other; and

a plurality of configurations each including a memory element and at least one yoke partially surrounding a line selected from the group consisting of one of said plurality of said first lines and one of said plurality of said second lines, said at least one yoke configured such that a magnetic flux through said at least one yoke is essentially closed by said memory element, said at least one yoke including a magetizable material with a relative permeability of at least 10;

said memory element being switched between a pair of states with a line selected from the group consisting one of said plurality of said first lines and one of said plurality of said second lines.

8. The memory cell array according to claim 7, wherein each one of said configurations includes a further yoke partially surrounding a different line selected from the group consisting of the one of said plurality of said first lines and the one of said plurality of said second lines;

said further yoke configured such that a magnetic flux through said further yoke is essentially closed by said memory

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element, said further yoke including a magetizable material with a relative permeability of at least 10.

9. The memory cell array according to claim 1, wherein said memory element includes at least one element or material selected from the group consisting of Fe, Ni, Co, Cr, Mn, Gd, Dy, Al_2O_3, NiO, HfO_2, TiO_2, NbO, and SiO_2; and

said first yoke includes at least one element selected from the group consisting of Fe, Ni, Co, Cr, Mn, Gd, and Dy.

10. A method for manufacturing a memory cell array, which comprises:

applying a first insulating layer to a carrier wafer;

producing a trench having side walls and a bottom in the first insulating layer;

producing a first yoke that adjoins the side walls of the trench and that adjoins the bottom of the trench, and producing the first yoke from a magnetizable material with a permeability of at least 10;

producing a first line in the trench;

producing a memory element with magnetoresistive effect above the first yoke and connecting the memory element to the first line; and

producing a second line above the memory element and connecting the second line to the memory element.

11. The method according to claim 10, which comprises:

in order to produce the first yoke, producing a second insulating layer having a trench formed with edges;

forming spacers made of a magnetizable material with a permeability of at least 10 on the edges of the trench formed in the second insulating layer;

producing the second line in the trench formed in the second insulating layer;

producing a yoke part from a magnetizable material with a permeability of at least 10; and

producing the yoke part to partially cover the second line above the memory element and connecting the yoke part to the spacers such that the spacers and the yoke part form a second yoke.

12. The method according to claim 10, which comprises forming a line selected from the group consisting of the first line and the second line by depositing a metal layer and by performing chemical-mechanical polishing.

13. The method according to claim 12, which comprises:

in order to produce the first yoke, applying a second insulating layer on the carrier wafer;

producing a trench having edges in the second insulating layer;

forming spacers, made of a magnetizable material with a permeability of at least 10, on the edges of the trench in the second insulating layer;

producing the second line in the trench in the second insulating layer;

producing a yoke part from a magnetizable material with a permeability of at least 10; and

producing the yoke part to partially cover the second line above the memory element and connecting the yoke part to the

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spacers such that the spacers and the yoke part form a second yoke.

14. The method according to claim 13, which comprises forming a line selected from the group consisting of the first line and the second line by depositing a metal layer and by performing chemical-mechanical polishing.